In the Claims:

1-2. (Canceled)

3. (Currently Amended) The vertical transistor architecture of claim 7 ~~claim 2~~, wherein the gate electrodes are arranged in the active trenches and wherein the gate electrodes of transistor cells which are adjacent in the x direction are connected to one another and form sections of word lines.

4. (Currently Amended) The vertical transistor architecture of claim 7 ~~claim 2~~, wherein the lower source/drain connection regions are in each case connected to a contiguous connection plate.

5. (Currently Amended) The vertical transistor architecture of claim 7 ~~claim 2~~, wherein the lower source/drain connection regions are in each case sections of a connection plate that is patterned at least in an upper region and is contiguous in a lower region.

6. (Canceled)

7. (Currently Amended) The A vertical transistor architecture ~~of claim 6, further~~ comprising:

an array of vertical transistor cells formed in a substrate and arranged in a transistor plane, in rows in an x direction, and in columns in a y direction perpendicular to the x direction;

an array of active trenches, wherein the active trenches separate the rows of transistor cells; and

an array of isolation trenches, wherein the isolation trenches separate the columns of transistor cells;

wherein active regions at least of transistor cells which are adjacent to one another in the x direction are connected to one another, whereby a charge carrier transport is made possible between the active regions of transistor cells which are adjacent in the x direction;

wherein the vertical transistor cells comprise:

respective lower source/drain connection region;

respective upper source/drain connection regions arranged above the lower source drain regions;

respective conductive channels disposed between the upper and lower source/drain connection regions; and

respective gate electrodes insulated from the active regions by a gate dielectric;

wherein the active regions are in each case sections of a contiguous layer body, wherein the contiguous body is patterned at least by the isolation trenches in an upper region, and wherein the contiguous body in a lower region connects the active regions of transistor cells that are adjacent to one another at least in the x direction;

wherein the vertical transistor architecture further comprises a plurality of layer bodies deposed in the transistor cell array in each case separated from one another by the active trenches.

8. (Original) The vertical transistor architecture of claim 7, wherein the layer bodies are lengthened in each case row by row into a connection array adjoining the transistor cell array.

9. (Original) The vertical transistor architecture of claim 8, wherein the layer bodies are connected to one another in the region of the connection array.

10. (Currently Amended) The vertical transistor architecture of claim 7 ~~claim 6~~, wherein the layer bodies are connected to a structure having a substrate potential.

11. (Currently Amended) The vertical transistor architecture of claim 7 ~~claim 6~~, wherein ~~the~~ a connection plate is patterned in an upper region by the active trenches extending along the x axis, wherein the lower source/drain connection regions are formed in the upper region of the connection plate in each case below the active regions, wherein the isolation trenches have a smaller depth than the active trenches, and wherein the layer bodies are formed contiguously row by row in each in a lower region below the isolation trenches.

12. (Original) The vertical transistor architecture of claim 11, wherein the isolation trenches are filled with an insulator material.

13. (Currently Amended) The vertical transistor architecture of claim 7 ~~claim 6~~, wherein the isolation trenches and the active trenches have an essentially identical depth, wherein the lower source/drain connection regions are formed in each case in an upper region of the connection plate below the active trenches, and wherein the layer bodies are formed contiguously row by

row in each case below the active regions and are separated from one another by the source/drain connection regions in a lower region.

14. (Currently Amended) The vertical transistor architecture of claim 7 ~~claim 6~~, wherein an upper region of the connection plate is patterned in the x direction and in the y direction, wherein a lower source/drain connection region delimited in the x direction and the y direction is in each case formed in the upper region of the connection plate, and wherein the active regions of transistor cells which are adjacent in the x direction and the y direction are formed contiguously by a single layer body which is patterned by the lower source/drain connection regions.

15. (Original) The vertical transistor architecture of claim 14, wherein the layer body is lengthened into a connection array adjoining the transistor cell array.

16. (Original) The vertical transistor architecture of claim 14, wherein the layer body is connected to a structure having a substrate potential.

17. (Currently Amended) The vertical transistor architecture of claim 7 ~~claim 2~~, wherein the active regions of the transistor cells have a cross-sectional area of essentially F^2 relative to a production-dictated minimum feature size F parallel to the transistor plane, and wherein the area requirement of a transistor cell is essentially 4 F^2.

18. (Currently Amended) The vertical transistor architecture of claim 7 ~~claim 2~~, further comprising a storage capacitor electrically connected to a source/drain connection region of each

selection transistor, whereby an array of memory cells each containing a vertical selection transistor is formed.

19. (Original) The vertical transistor architecture of claim 18, wherein the selection transistors are connected to the assigned storage capacitor in each case at an upper source/drain connection region.

20. (New) A vertical transistor architecture comprising:

an array of vertical transistor cells formed in a substrate and arranged in a transistor plane, in rows in an x direction, and in columns in a y direction perpendicular to the x direction;

an array of active trenches, wherein the active trenches separate the rows of transistor cells; and

an array of isolation trenches, wherein the isolation trenches separate the columns of transistor cells;

wherein active regions at least of transistor cells which are adjacent to one another in the x direction are connected to one another, whereby a charge carrier transport is made possible between the active regions of transistor cells which are adjacent in the x direction;

wherein the vertical transistor cells comprise:

respective lower source/drain connection region;

respective upper source/drain connection regions arranged above the lower source drain regions;

respective conductive channels disposed between the upper and lower source/drain connection regions; and

respective gate electrodes insulated from the active regions by a gate dielectric;

wherein the active regions are in each case sections of a contiguous layer body, wherein the contiguous body is patterned at least by the isolation trenches in an upper region, and wherein the contiguous body in a lower region connects the active regions of transistor cells that are adjacent to one another at least in the x direction; and

wherein a connection plate is patterned in an upper region by the active trenches extending along the x axis, wherein the lower source/drain connection regions are formed in the upper region of the connection plate in each case below the active regions, wherein the isolation trenches have a smaller depth than the active trenches, and wherein the layer bodies are formed contiguously row by row in each in a lower region below the isolation trenches.

21. (New) The vertical transistor architecture of claim 20, wherein the isolation trenches are filled with an insulator material.

22. (New) A vertical transistor architecture comprising:

an array of vertical transistor cells formed in a substrate and arranged in a transistor plane, in rows in an x direction, and in columns in a y direction perpendicular to the x direction;

an array of active trenches, wherein the active trenches separate the rows of transistor cells; and

an array of isolation trenches, wherein the isolation trenches separate the columns of transistor cells;

wherein active regions at least of transistor cells which are adjacent to one another in the x direction are connected to one another, whereby a charge carrier transport is made possible

between the active regions of transistor cells which are adjacent in the x direction;

wherein the vertical transistor cells comprise:

respective lower source/drain connection region;

respective upper source/drain connection regions arranged above the lower source drain regions;

respective conductive channels disposed between the upper and lower source/drain connection regions; and

respective gate electrodes insulated from the active regions by a gate dielectric;

wherein the active regions are in each case sections of a contiguous layer body, wherein the contiguous body is patterned at least by the isolation trenches in an upper region, and wherein the contiguous body in a lower region connects the active regions of transistor cells that are adjacent to one another at least in the x direction; and

wherein an upper region of a connection plate is patterned in the x direction and in the y direction, wherein a lower source/drain connection region delimited in the x direction and the y direction is in each case formed in the upper region of the connection plate, and wherein the active regions of transistor cells which are adjacent in the x direction and the y direction are formed contiguously by a single layer body which is patterned by the lower source/drain connection regions.

23. (New) The vertical transistor architecture of claim 22, wherein the layer body is connected to a structure having a substrate potential.